What is claimed is:

1. A forward converter, comprising:

a transformer having a primary winding and a secondary winding;

a power switch connected in series with said transformer and coupled to an input power source, said power switch capable of being alternately switched between an on period and an off period as a function of a PWM signal comprising pulses generated by a PWM circuit and such that an AC voltage is generated across said secondary winding in response thereto;

an output filter operative to provide a substantially constant DC voltage to an output load;

a forward rectifier having a control input and being operative to provide a forward conduction path between said secondary winding and said output filter during said on period;

a free-wheeling synchronous rectifier having a control input and being operative to provide a second conduction path for maintaining current to said output filter during said off period; and

a control circuit coupled to said control input of said free-wheeling synchronous rectifier for controlling the state thereof, said control circuit receiving a clock signal varying between an upper voltage and a lower voltage and having a frequency equal to or greater than said PWM signal, comprising:

a reference circuit for generating a PWM reference signal by causing the trailing edge of said PWM signal to decrease in voltage at a predetermined rate such that said PWM reference signal drops below and remains below said lower voltage if the next pulse of said PWM signal has not been generated;

a comparator circuit for comparing said PWM reference signal to said clock signal and for generating an output signal as a function thereof such that said output signal is on when said PWM reference signal is below said lower voltage; and

a driver circuit responsive to said output signal and said PWM signal so as to turn off said free-wheeling synchronous rectifier when said output signal is on and so as to enable said PWM signal to control said free-wheeling synchronous rectifier when said output signal is off.

2. The forward converter of Claim 1, wherein said reference circuit is for generating a PWM reference signal by causing the trailing edge of said PWM signal to decrease in voltage at

a predetermined rate such that said PWM reference signal drops below and remains below said lower voltage if the leading edge of the next pulse of said PWM signal has not been generated.

3. The forward converter of Claim 1, wherein if said PWM reference signal drops below and remains below said lower voltage of said clock signal, said driver circuit turns off said free-wheeling synchronous rectifier within one cycle of said clock signal after said PWM reference signal drops below said lower voltage.

4. The forward converter of Claim 1, wherein said reference circuit is for generating a PWM reference signal by causing the trailing edge of said PWM signal to decrease in voltage at a predetermined rate such that said PWM reference signal drops below and remains below the amplitude of said clock signal if the next pulse of said PWM signal has not been generated.

5. The forward converter of Claim 4, wherein if said PWM reference signal drops below and remains below the amplitude of said clock signal, said driver circuit turns off said free-wheeling synchronous rectifier within one cycle of said clock signal after said PWM reference signal drops below the amplitude of said clock signal.

6. The forward converter of Claim 1, wherein said clock signal varies from 1 volt to 3 volts.

7. The forward converter of Claim 1, wherein said clock signal has a frequency that is about twice that of said PWM signal.

8. The forward converter of Claim 1, wherein, said free-wheeling synchronous rectifier is a MOSFET.

9. The forward converter of Claim 1, wherein said reference circuit comprises:

a first diode coupled between the output of said PWM circuit and a first node, and

an RC circuit for causing the trailing edge of said PWM signal to decay at a predetermined rate according to a predetermined RC time constant such that said PWM reference signal drops below and remains below said lower voltage if the next pulse of said PWM signal

has not been generated, said RC circuit comprising a first resistor connected in parallel with a first capacitor between said first node and ground.

10. The forward converter of Claim 1, wherein said comparator circuit comprises a comparator having a positive input and a negative input, said PWM reference signal being coupled to said negative input and said clock signal being coupled to said positive input.

11. The forward converter of Claim 1, further comprising a voltage divider coupled across the output of said converter for generating a feedback signal responsive thereto, said feedback signal being coupled to said PWM circuit.

12. The forward converter of Claim 1, wherein said driver circuit comprises:

an OR gate having a first and second input and an output, said first input being coupled to the output of said PWM controller, said second input being coupled to the output of said comparator circuit.

13. The forward converter of Claim 12, said driver circuit further comprising:

an inverter and a buffer connected in series between the output of said OR gate and said control input of said free-wheeling synchronous rectifier.

14. The forward converter of Claim 12, wherein said output filter comprises an inductor in series with a capacitor, said capacitor being connected across the output of said converter, and wherein said free-wheeling synchronous rectifier is a MOSFET having a source, drain and gate, the drain of said free-wheeling synchronous rectifier is coupled to said inductor, the source of said free-wheeling synchronous rectifier is coupled to ground; said driver circuit further comprising:

a driver rectifier coupled between the control input of said free-wheeling synchronous rectifier and ground and having a control input coupled to said output of said OR gate.

15. The forward converter of Claim 14, said driver circuit further comprising a resistor connected in series between the control input of said free-wheeling synchronous rectifier and ground.

16. The forward converter of Claim 1, wherein said power switch is a first power switch and said primary winding having a first end and a second end, said forward converter further comprising a second power switch, said first power switch connected in series between said first end and one of said input terminals, said second power switch connected in series through a resistor between said second end and the other of said input terminals; a first diode connected in series with said resistor between said first end and the other of said input terminals; a second diode connected in series between said second end and the first one of said input terminals, such that said first and second diodes provide a path for resetting said transformer.

17. The forward converter of Claim 1, further comprising an auxiliary winding magnetically coupled to said primary winding such that said AC voltage is generated across said auxiliary winding in response to the switching of said power switch, one end of said auxiliary winding being coupled through a first diode to the control input of said forward rectifier and the other end of said auxiliary winding being coupled to ground; a second diode coupled between the junction of said output filter and said secondary winding and the control input of said forward rectifier; and a third diode and a resistor connected in parallel between the control input of said forward rectifier and ground.

18. The forward converter of Claim 1, wherein said free-wheeling synchronous rectifier is a MOSFET having a source, a drain and a gate, the drain of said free-wheeling synchronous rectifier being coupled to said output filter, the source of said free-wheeling synchronous rectifier being coupled to ground; said forward converter further comprising a second resistor and a fourth and fifth diode connected in series between the control input of said free-wheeling synchronous rectifier and ground, the second resistor connected in series with the fourth diode between a second node and the control input of said free-wheeling synchronous rectifier, said fifth diode having an anode connected to ground and a cathode connected to the anode of the fourth diode at said second node, and a third resistor connected between the control input of said

free-wheeling synchronous rectifier and ground, an auxiliary winding magnetically coupled to said primary winding such that said AC voltage is generated across said auxiliary winding in response the switching of said switch, one end of said auxiliary winding being coupled to the control input of said forward rectifier and the other end of said auxiliary winding being coupled to said second node, a sixth diode coupled between the junction of said inductor and said secondary winding and the control input of said forward rectifier, a seventh diode and a fourth resistor connected in parallel between the control input of said forward rectifier and ground.

19. A buck converter for converting said input DC voltage to a regulated output DC voltage, said buck converter having an input terminal to which an input DC voltage is coupled and an output terminal where the output DC voltage is provide, comprising:

an output filter operative to provide a substantially constant DC voltage to an output load;

a power switch connected in series between said input terminal and said output filter; said power switch capable of being alternately switched between an on period and an off period as a function of a PWM signal comprising pulses generated by a PWM circuit;

a free-wheeling synchronous rectifier having a control input and being operative to provide a second conduction path for maintaining current to said output filter during said off period;

a control circuit coupled to said control input of said free-wheeling synchronous rectifier for controlling the state thereof, said control circuit receiving a clock signal varying between an upper voltage and a lower voltage and having a frequency equal to or greater than said PWM signal, comprising:

a reference circuit for generating a PWM reference signal by causing the trailing edge of said PWM signal to decrease in voltage at a predetermined rate such that said PWM reference signal drops below and remains below said lower voltage if the next pulse of said PWM signal has not been generated;

a comparator circuit for comparing said PWM reference signal to said clock signal and for generating an output signal as a function thereof such that said output signal is on when said PWM reference signal is below said lower voltage; and

a driver circuit responsive to said output signal and said PWM signal so as to turn off said free-wheeling synchronous rectifier when said output signal is on and so as to enable

said PWM signal to control said free-wheeling synchronous rectifier when said output signal is off.

20. The buck converter of Claim 19, further comprising a voltage divider coupled across the output of said converter for generating a feedback signal responsive thereto, said feedback signal being coupled to said PWM circuit.

21. The buck converter of Claim 19, said driver circuit further comprising an inverter and a buffer connected in series between the output of said OR gate and said control input of said free-wheeling synchronous rectifier.

22. A power converter comprising:

a power switch capable of being alternately switched between an on period and an off period as a function of a PWM signal comprising pulses generated by a PWM circuit;

an output filter operative to provide a substantially constant DC voltage to an output load;

a synchronous rectifier having a control input and being operative to provide a second conduction path for maintaining current to said output filter during the off period of said converter; and

a control circuit coupled to said control input of said free-wheeling synchronous rectifier for controlling the state thereof, said control circuit receiving a clock signal varying between an upper voltage and a lower voltage and having a frequency equal to or greater than said PWM signal, comprising:

a reference circuit for generating a PWM reference signal by causing the trailing edge of said PWM signal to decrease in voltage at a predetermined rate such that said PWM reference signal drops below and remains below said lower voltage if the next pulse of said PWM signal has not been generated,

a comparator circuit for comparing said PWM reference signal to said clock signal and for generating an output signal as a function thereof such that said output signal is on when said PWM reference signal is below said lower voltage, and

a driver circuit responsive to said output signal and said PWM signal so as to turn off said free-wheeling synchronous rectifier when said output signal is on and so as to enable

said PWM signal to control said free-wheeling synchronous rectifier when said output signal is off.

23. A method of controlling the state of a synchronous rectifier in a power converter, said power converter having an input terminal to which an input DC voltage is coupled and an output terminal where the output DC voltage is provided, comprising the steps of:

receiving a PWM signal from a PWM controller;

receiving a clock signal varying between an upper voltage and a lower voltage and having a frequency equal to or greater than said PWM signal;

generating a PWM reference signal by causing the trailing edge of said PWM signal to decrease in voltage at a predetermined rate such that said PWM reference signal drops below and remains below said lower voltage if the next pulse of said PWM signal has not been generated;

generating an output signal as a function of said PWM reference signal and said clock signal such that said output signal is on when said PWM reference signal is below said lower voltage;

turning off said free-wheeling synchronous rectifier when said output signal is on; and

enabling said PWM signal to control said free-wheeling synchronous rectifier when said output signal is off.

24. A power system having a plurality of DC-DC converter modules, each having an input terminal to which an input DC voltage is coupled and an output terminal where the output DC voltage is provided, said converter modules being connected in parallel through their output terminals, each said converter module comprising:

a buck converter for converting said input DC voltage to a regulated output DC voltage, said buck converter having an input terminal to which an input DC voltage is coupled and an output terminal where the output DC voltage is provide, said buck converter comprising an output filter operative to provide a substantially constant DC voltage to an output load, a power switch connected in series between said input terminal and said output filter, said power switch capable of being alternately switched between an on period and an off period as a function of a PWM signal comprising pulses generated by a PWM circuit, a free-wheeling synchronous rectifier having a control input and being operative to provide a second conduction path for

maintaining current to said output filter during said off period, a voltage divider coupled across the output of said converter for generating a feedback signal responsive thereto, said feedback signal being coupled to said PWM circuit, and a control circuit coupled to said control input of said free-wheeling synchronous rectifier for controlling the state thereof, said control circuit receiving a clock signal varying between an upper voltage and a lower voltage and having a frequency equal to or greater than said PWM signal, said control circuit comprising a reference circuit for generating a PWM reference signal by causing the trailing edge of said PWM signal to decrease in voltage at a predetermined rate such that said PWM reference signal drops below and remains below said lower voltage if the next pulse of said PWM signal has not been generated, a comparator circuit for comparing said PWM reference signal to said clock signal and for generating an output signal as a function thereof such that said output signal is on when said PWM reference signal is below said lower voltage, and a driver circuit responsive to said output signal and said PWM signal so as to turn off said free-wheeling synchronous rectifier when said output signal is on and so as to enable said PWM signal to control said free-wheeling synchronous rectifier when said output signal is off;

a current sense circuit, coupled to each said converter module, for detecting the output current of said converter module and for generating a current sense signal that is a function thereof;

a parallel sense circuit for generating a current share signal at a common current sharing bus that is a function of each of said current sense signals; and

a parallel control circuit coupled to said PWM circuit of each said converter module for adjusting the output power of that respective converter module as a function of that converter module's current sense signal and said current share signal.

25. A power system having a plurality of DC-DC converter modules, each having an input terminal to which an input DC voltage is coupled and an output terminal where the output DC voltage is provided, said converter modules being connected in parallel through their output terminals, each said converter module comprising:

a forward converter for converting said input DC voltage to a regulated output DC voltage comprising a transformer having a primary winding and a secondary winding, a power switch connected in series with said transformer and coupled to an input power source, said

power switch capable of being alternately switched between an on period and an off period as a function of a PWM signal comprising pulses generated by a PWM circuit and such that an AC voltage is generated across said secondary winding in response thereto, an output filter operative to provide a substantially constant DC voltage to an output load, a forward rectifier having a control input and being operative to provide a forward conduction path between said secondary winding and said output filter during said on period, a free-wheeling synchronous rectifier having a control input and being operative to provide a second conduction path for maintaining current to said output filter during said off period, a voltage divider coupled across the output of said converter for generating a feedback signal responsive thereto, said feedback signal being coupled to said PWM circuit, a control circuit coupled to said control input of said free-wheeling synchronous rectifier for controlling the state thereof, said control circuit receiving a clock signal varying between an upper voltage and a lower voltage and having a frequency equal to or greater than said PWM signal, said control circuit comprising a reference circuit for generating a PWM reference signal by causing the trailing edge of said PWM signal to decrease in voltage at a predetermined rate such that said PWM reference signal drops below and remains below said lower voltage if the next pulse of said PWM signal has not been generated, a comparator circuit for comparing said PWM reference signal to said clock signal and for generating an output signal as a function thereof such that said output signal is on when said PWM reference signal is below said lower voltage, and a driver circuit responsive to said output signal and said PWM signal so as to turn off said free-wheeling synchronous rectifier when said output signal is on and so as to enable said PWM signal to control said free-wheeling synchronous rectifier when said output signal is off;

a current sense circuit, coupled to each said converter module, for generating a current sense signal as a function of the current sensed through said power switch;

a parallel sense circuit for generating a current share signal at a common current sharing bus that is a function of each of said current sense signals; and

a parallel control circuit coupled to said PWM circuit of each said converter module for adjusting the output power of that respective converter module as a function of that converter module's current sense signal and said current share signal.